Design Of Novel High Speed and Low Area 15:4 Compressors Using Xilinx Tool

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Abstract

Current day technology requires a high speed and low power architectures.In modelling basic arithmetic circuit ,adder plays a major role in applications like multipliers and digital signal processors.To obtain better results w.r.to high speed and lower power consumption,optimization schems are employed at all levels of abstraction.In this paper optimizations are done at logic level by replacing XOR gates with multiplexers for better power and delay products,optimizations at electrical level for the reduction of internal capacitances and optimization at physical level to reduce area when compared to the manual design approach.Digital Schematic and Microwind tool are used to optimize design for low power ,low area and automatic conversion of layout with better results when compared to manual layout design In this paper xilinx implementation is done instead of microwind and digital schematic implementation.

KEYWORDS—Compressors,3-2 compressor,4-2 compressor, higher order compressors,Xilinx tool implementation.

I. Introduction

With the advancement of technology and portable devices such as mobile electronic gadgets which are ready for applications such as smartphones,portable video games and tablets demands low power,low area and higher performance.And these parameters are contradictory to each other hence a tradeoff is needed between them to obtain optimum solutions.So optimization efforts are needed at all levels of abstractions to obtain better outcomes[1].Traditional standard cell based design approach limits the optimization efforts as the standard cell library contains limited logic resources and sizing versions. Inthis scenario logic library free approach gives a possible solutions [2].Xilinx tool used for automatic generation of synthesis resultss gate level equivalents.Results shows that these extracted models are better interms of performance compared their manual counterparts.This paper is organized as five sections.First section gives introduction,adder compressors are presented along with their architectures are presented in section2, implementation results of different adder /compressors are presented in section 3 and final conclusion in section 4.

2. Adder Compressor Architectures

Todays arithmetic and digital signal processing circuits require multipliers for low power and high performance applications uses adder compressor circuits [5].Multipilers have following three modules.

1. Generation of partial products
2. Accumulation of partial products and
3. Final addition.

Partial product accumulation stage is the major source of power, delay and area [6].To reduce the number of partial products adder compressors are more helpful in critical path length analysis.

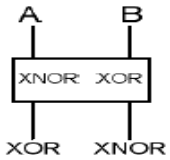

Figure1: Block schematic of XOR-XNOR design

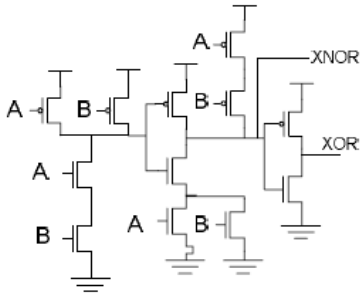

Figure2: CMOS realization of XOR-XNOR design

Compressors basically consist of two modules, XOR –XNOR complex gates and multiplexers (MUX). Above Figure1 shows block schematic of XOR-XNOR implementation and figure2 shows CMOS implementation of the compressors.Different design approaches for 4-2 and 5-2 compressors are presented in[6].It shows different ways to implement adder compressors based on different logic styles with same architecture mentioned in figure1 and figure2.Implementation results shows better results for some combinations in terms of delay and power.Figure2(a) shows block schematic of multiplexer and figure2(b) shows CMOS implementation of mux with a buffer at output .Figure3(a) presents a beeter style of compressor design which is developed based on Transmission gate and buffer at output than figure3(b).

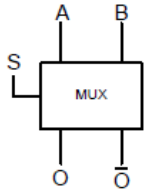

Figure:2(a):Block schematic of MUX

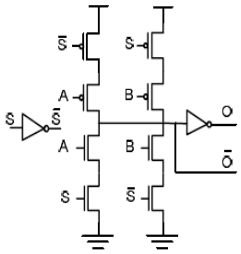

Figure:2(b):CMOS Implementation of MUX with buffered output

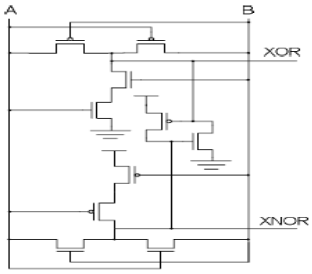

Figure:3(a):CMOS realization of XOR –XNOR gates.

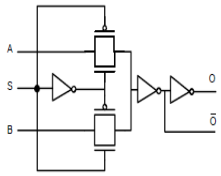

Figure:3(b):MUX with transmission gate and buffer output.

A novel architecture is presented in [7].In this style emphasis lay on the usage of multiplexers instead of XOR gates.For the XOR-XNOR modules in this we use the traditional CMOS logic style and for the MUX module we use Transmission gate with output taken across buffer for better results.

2.1.3-2 Compressors

Figure4 (a) shows adder compressor which generates two outputs sum and carry bits by accepting three input bits A, B, C. Followed by truth table of compressor in table1.

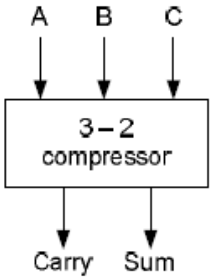

Figure4(a):Block schematic of 3-2 Compressor

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 1: Truth Table of 3-2 Compressor

Expression of 3-2 compressor is given by

A+B+C= sum + (2* carry) (1)

The traditional architecture is shown in figure5 (a) and is designed by using CMOS logic style of the XOR-XNOR module and Mux modules with transmission gates.

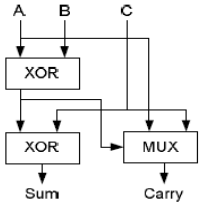

Figure5(a):XOR-MUX Implementation

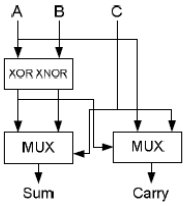

Figure5 (b):XOR-XNOR Implementation

Altered expressions are given by

$$Sum = A \oplus B \oplus C \qquad (2)$$

$$Carry = (A \oplus B) * C + \overline{(A \oplus B)} * A \qquad (3)$$

Figure5(b) shows enhanced version of 3-2 compressor architecture .Altered expressions are given by

$$Sum = (A \oplus B) * \overline{C} + \overline{(A \oplus B)} * C \qquad (4)$$

$$Carry = (A \oplus B) * C + \overline{(A \oplus B)} * A \qquad (5)$$

2.2:4-2 Compressor

The 4-2 compressor generates '3' outputs sum,carry and Cout and accepts '5' inputs A,B,C,D,Cin as shown in figure6(a).Cin is the output from previous lower significant compressor and Cout is the output of the compressor in the next significant stage.The general approach to implement 4-2 compressors are by using two full adders connected serially as shown in figure 6(b).

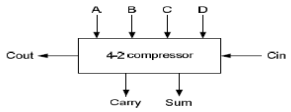

Figure 6(a):Block schematic of 4-2 compressors

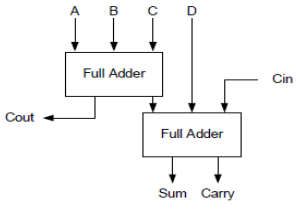

Figure 6(b):Block schematic of 4-2 compressors developed using full adders.

The 4-2 compressor expression is given by

$$A+B+C+D+Cin = Sum+2*(Carry+Cout) \quad (6)$$

Figure7 shows the two architectures implemented in this work .Figure7 (a) shows the traditional architecture which is developed based on CMOS logic styleof XOR-XNOR and MUX modules similar to 3-2 Compressors.

$$Sum = A \oplus B \oplus C \oplus D \oplus Cin \quad (7)$$

$$Cout = (A \oplus B) * C + \overline{(A \oplus B)} * A \quad (8)$$

$$Carry = (A \oplus B \oplus C \oplus D) * Cin + \overline{(A \oplus B \oplus C \oplus D)} * D \quad (9)$$

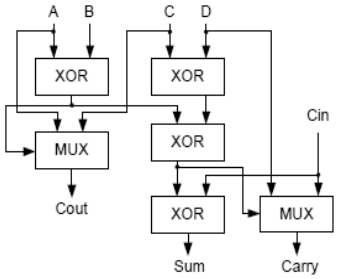

Figure7(a):Realization of 4-2 using XOR-MUX style.

Figure7(b) shows the enhanced model of 4-2 compressor architecture .This uses the XOR-XNOR and MUX using transmission gate module presented in Figure 3(a) and 3(b).

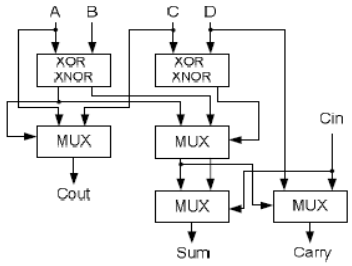

Figure7(b): CMOS logic styleof XOR-XNOR and MUX modules of 4-2 compressor

This architecture is governed by the following equations

$$Sum = ((A \oplus B) * (\overline{C \oplus D}) + (\overline{A \oplus B}) * (C \oplus D)) * Cin + \overline{((A \oplus B) * (\overline{C \oplus D}) + (\overline{A \oplus B}) * (C \oplus D)) * Cin} \quad (10)$$

$$Cout = (A \oplus B) * C + \overline{(A \oplus B)} * A \quad (11)$$

$$Carry = (A \oplus B \oplus C \oplus D) * Cin + \overline{(A \oplus B \oplus C \oplus D)} * D \quad (12)$$

2.3:5-2 Compressors

The block diagram of 5-2 compressor is given in figure8 has seven inputs and four outputs . '5' inputs i1, i2, i3, i4, i5 are primary inputs and two other inputs Cin1 and Cin2.

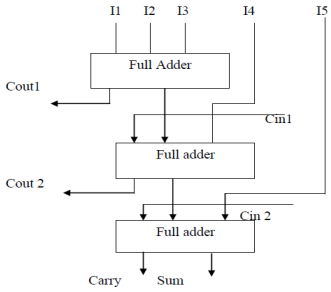

Figure 8: Block Schematic of 5-2 compressors

Instead of conventional 5-2 compressors we propose a novel scheme based on counter logic and is presented in Figure 9.

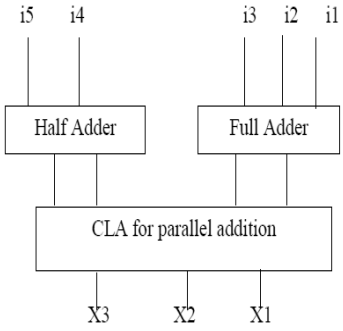

Figure 9: Counter based 5-2 Compressors

The counting limit of this compressor is zero to five. The realizations of 6-3 and 7-3 compressors are almost similar like 5-3 compressor; only one more input to be added to 6-3 compressor and two inputs to be added to 7-3 compressor.The novel 6-3, 7-3 can be designed by using one 4-3 compressors and one full adder and parallel adders.Figure10a. shows this approach.Counter logic used in Compressors are as follows ,If no input is '1' then output is "000" with decimal equivalnt'0' and if any one input is '1' then output is "001" with decimal equivalent '1' and if any two inputs are '1' then output is "010" with decimal equivalent '2' similarly upto '5'. The proposed higher order compressors, 8-4 and 9-4 presented in figure 11a, figure 11b respectively gives better performance than the lower order compressors in terms of speed and area but the delay can be further reduced by using 8-4 and 9-4 compressors.

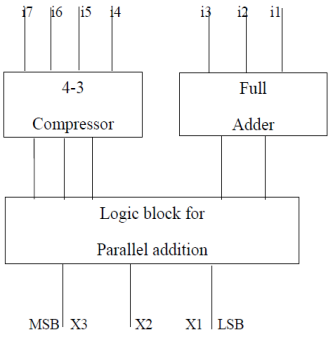

Figure10a:6-3 Compressor based on 4-3 compressor

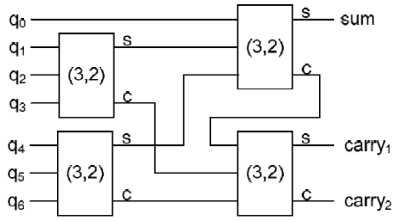

Figure10b:7-3 Compressor based on 3-2 compressor

A correct combination of adder has chosen to develop an efficient 8-4 and 9-4 compressor. Structure of 8-4 and 9-4 Compressors Using full and half adder shown in Figure. 11a, shows that 8-4 compressor has 8 inputs (I0-I7) and four outputs (X1- X4). This compressor uses counter property so that, output of compressor gives number of 1's at input.For example,if all input bits are 1, then output of the compressor is "1000". Figure 11b shows MUX based design of 8-4 compressor.

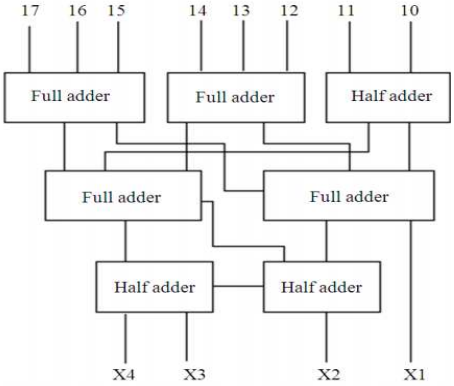

Figure: 11a:8-4 Compressor using adders

The structures shown in figure 11c and figure 11d realized with the help of multiplexer in order to get the better result in terms of power dissipation and energy delay product. Figure 11c and figure 11d shows the implementation of 8-4 compressors and 9-4 compressors.

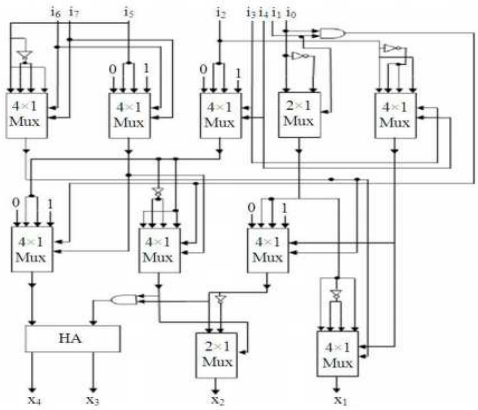

Figure 11b: MUX based design of 8-4 compressor.

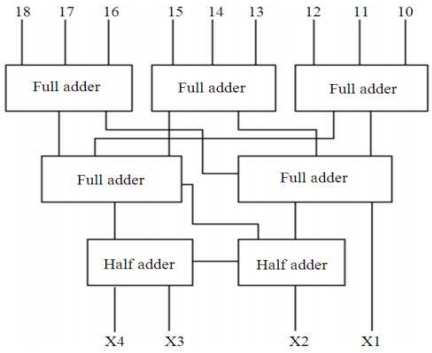

Figure: 11c :9-4 Compressor using adders

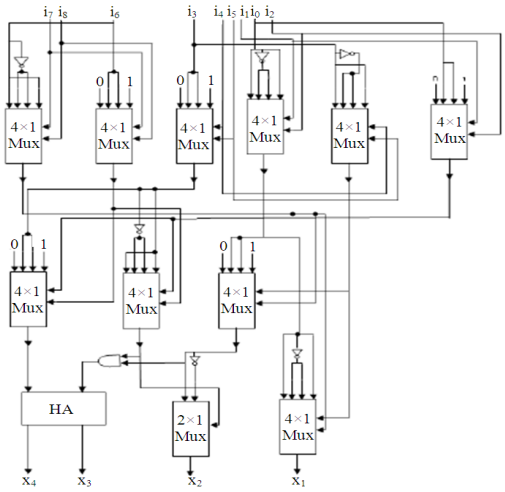

Figure: 11d :9-4 Compressor using MUX

In a multiplexer the selected part is only the active, leaving the rest in idle mode.Thereby saving substantial amount of power and therefore reducing the energy delay product by many folds. Different types of compressors are used to compute the partial product.Partial products are added in five stages. Proper pairs of compressors/adders have been used in order to reduce the vertical critical path. High order compressors have less gate count and occupy less area than conventional compressors and consume more power than low order compressor. 15-4 Compressor [11] has been designed using the proposed 5-3 Compressor.

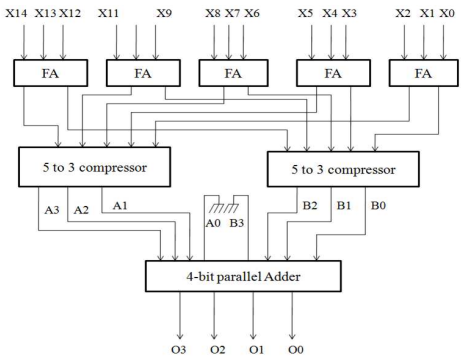

Figure 12:15-4 Compressor based on Proposed 5-3 compressors and parallel adders

The architectural design of the proposed 15-4 Compressor is shown in figure 13. The architecture is based on a bit sliced addition technique. The 15 input bits are divided five groups of three bits each. The 3 input bits in each group are compressed into 2 bits in the first stage using a full adder. The outputs of the Compressor are sent to a 4 bit parallel adder that has been suitably optimized according to the design requirements. Since the 5-3 Compressor that computes the sum of the carry outputs of the full adders in the first stage produces a result that has twice the weight of the output of the other Compressor, hence the Compressor output is sent to the parallel adder after being appropriately left shifted. Since least significant bit of the one set of 4 bits is zero and the most significant bit of the other set of 4 bits is zero,hence the adder design is suitably optimized .Compressor has been designed using the proposed 5-3 Compressor. The architectural design of the proposed 15-4 Compressor is shown in figure 13. The architecture is based on a bit sliced addition technique. The 15 input bits are divided five groups of three bits each. The 3 input bits in each group are compressed into 2 bits in the first stage using a full adder.The outputs of the Compressor are sent to a 4 bit parallel adder that has been suitably optimized according to the design requirements.

3. Implementation

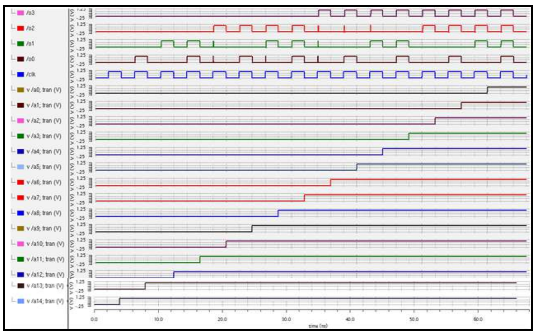

Figure 13: Simulation Results of 15-4 Compressor

Results shown in figure 13,compress 15 input bits into four output bits.``

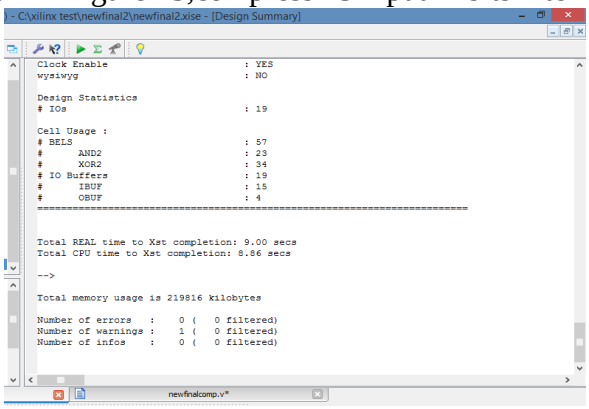

Figure14a: Synthesis results of 15-4 compressor using adder.

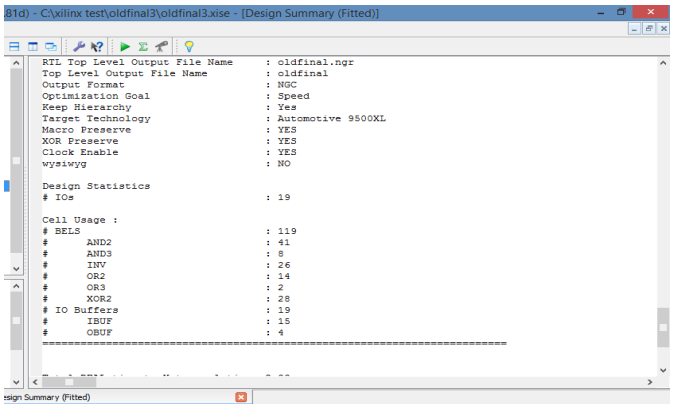

Figure 14b: Synthesis results of 15-4 compressor using 4-1 MUX.

From figure 14a, figure 14b it can be observed that the number of gates in conventional method (15-4 Compressor using 4-1 multiplexer) is 119. But when this 15-4 compressor is executed in the new proposed method (15-4 Compressor using Adders) the number of gates decreases to 57. The number of gates is approximately reduced by 50%.

4. Future scope

With the help of similar architecture higher order compressors can be modeled. The architectures of 3-2 , 4-2 ,5-5 ,6-3 ,7-3 ,8-4 ,9-4 ,15-4 compressors are analyzed using 2 logic styles for the XOR-XNOR and MUX modules.According to previous works [4], the layouts generated by different tools reduce the power consumption of the circuits. Optimization techniques for low power should be applied in all abstraction levels, and this work the logic, electrical and physical levels are explored.As future works we are already working on applying these optimizations on a 65 nm process, and analyze the circuit sensitivity to PVT (Process, Voltage and Temperature) variations.

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